WHAT IS CLAIMED IS:

1. A semiconductor device having a plurality of wiring layers on which a dummy pattern and an actual pattern are arranged,

wherein a position of a center point of said dummy pattern arranged on an (N+1)th wiring layer (N=natural number) is different from at least one of followings: a position of a center point of said dummy pattern arranged on an Nth wiring layer, and a position on a center line of said actual pattern.

2. The semiconductor device according to claim 1,

wherein positions of center points of said dummy patterns on said plurality of wiring layers vary for respective wiring layers.

3. A semiconductor device having a plurality of wiring layers on which a dummy pattern and an actual pattern are arranged,

wherein said dummy pattern has a rectangular shape and is arranged by rotating a given angle in a direction in which said actual pattern extends.

4. The semiconductor device according to claim 3,

wherein longer sides of said dummy pattern extend in a same direction as said actual pattern which is perpendicularly wired extends.

5. The semiconductor device according to claim 3,

wherein longer sides of said dummy pattern extend perpendicularly to the direction in which said actual pattern extends.

6. The semiconductor device according to claim 5, wherein said actual pattern is perpendicularly wired.

7. The semiconductor device according to claim 3, wherein positions of center points of said dummy patterns of said plurality of wiring layers vary for respective wiring layers.

8. The semiconductor device according to claim 3, wherein positions of center points of said dummy patterns of said plurality of wiring layers vary for respective wiring layers and respective longer sides of said dummy patterns on different wiring layers extend parallel to each other.

9. The semiconductor device according to claim 3, wherein respective longer sides of said dummy patterns on adjacent wiring layers extend perpendicularly to each other.

10. A pattern generation method for a semiconductor device,

wherein a position of a center point of said dummy pattern arranged on an (N+1)th wiring layer (N=natural number) is made different from at least one of followings: a position of a center point of said dummy pattern arranged on an Nth wiring layer, and a position on a center line of an actual pattern.

11. A pattern generation method for a semiconductor device,

wherein a dummy pattern on an (N+1)th wiring

layer is arranged so that a center point thereof does not overlap center points of dummy patterns on first to Nth wiring layers (N=natural number).

12. A pattern generation method for a semiconductor device,

wherein a dummy pattern having a rectangular shape is arranged by rotating a given angle to an extending direction of an actual pattern on the same wiring layer on which the actual pattern is arranged.

13. The pattern generation method for a semiconductor device according to claim 12,

wherein the dummy pattern is arranged so that longer sides thereof extend in the same direction as the actual pattern, which is perpendicularly wired, extends.

14. The pattern generation method for a semiconductor device according to claim 12,

wherein the dummy pattern is arranged so that the longer sides thereof extend perpendicularly to a direction in which the actual pattern being perpendicularly wired extends.

15. The pattern generation method for a semiconductor device according to claim 12,

wherein the dummy pattern is arranged so that long sides thereof extend perpendicularly to that of the dummy patterns on the adjacent wiring layers.